REMARKS/ARGUMENTS

Favorable consideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 20-25 are pending in this case, with Claims 1-19 cancelled and Claims 20, 22, 24 and 25 having been amended by way of the present Preliminary Amendment.

In the Office Action of May 5, 2003 for parent Application Serial No. 09/699,481, filed October 31, 2000, Claims 20-22 and 25 were rejected under 35 U.S.C § 102(b) as being anticipated by Applicants' disclosure of Posch et al (IEEE Transactions on Parallel and Distributed Systems); Claims 1-25 were rejected under 35 U.S.C. § 112, second paragraph; and Claims 1-19, 23 and 24 were indicated as containing allowable subject matter.

Applicants acknowledge with appreciation the indication of allowance for Claims 23 and 24 in the Office Action of May 5, 2003 for parent Application Serial No. 09/699,481.

Claims 20-25 were cancelled from parent Application Serial No. 09/699,481 to permit the allowable Claims 1-19 to pass to issuance. Thus, a discussion of Claims 1-19 is moot.

Claims 20, 22, 24 and 25 are hereby amended to correct the informalities noted in the Official Action of May 5, 2003. No new matter is added. Thus, Applicants believe the rejection under 35 U.S.C. § 112, second paragraph has been overcome.

Claim 20 is further amended to recite that the correction term calculation unit sequentially calculates the correction term in units of bits, *each bit from the sequence being fed to the modular arithmetic operation individually for a corresponding sequential calculation*. Support for this amendment is found in Applicants' originally filed specification.[1] No new matter is added.

Briefly recapitulating, amended Claim 20 is directed to a modular arithmetic apparatus, comprising a plurality of product-sum circuits configured to receive a plurality of

[1] Specification, page 22, line 20 – page 23, line 4; Figure 3.

base elements and execute a modular arithmetic operation. The apparatus also comprises a correction term calculation unit configured to receive the plurality of base elements in parallel to the plurality of product-sum circuits and to calculate a sequence of bits of a correction term to be used in the modular arithmetic operation. The correction term calculation unit sequentially calculates the correction term in units of bits, each bit from the sequence being fed to the modular arithmetic operation individually for a corresponding sequential calculation. Each of the product-sum circuits sequentially uses the correction term calculated by the correction term calculation unit and performs one of a base conversion operation or base extension operation.

Posch et al teaches a correction term calculation unit that may used with a modular arithmetic unit. However, Posch et al does not teach or suggest a correction term calculation unit that sequentially calculates the correction term in units of bits, *each bit from the sequence being fed to the modular arithmetic operation individually for a corresponding sequential calculation* as recited in Applicants' amended Claim 20. As noted in Applicants' originally filed specification,[2] "the implementation of Posch et al cannot be fed back until the correction term is completely calculated." Thus, the Posch transmission bus width for transmitting the correction term to the product-sum circuits is not r bits but is $(r + \log_2 n)$ bits, requiring a larger and more complex circuit than is required for Applicants' claimed invention.[3] Therefore, Applicants submit the inventions defined by Claim 20, and all claims depending therefrom, are neither anticipated nor rendered obvious by the asserted prior art for at least the reasons stated above.[4]

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[2] Specification, page 8, line 21 – page 9, line 6.
[3] Specification, page 9, lines 2-25.
[4] MPEP § 2142 "...the prior art reference (or references when combined) must teach or suggest **all** the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)."

Accordingly, examination on the merits of Claims 20-25 is believed to be in order, and an early and favorable action is respectfully requested.

Respectfully submitted,

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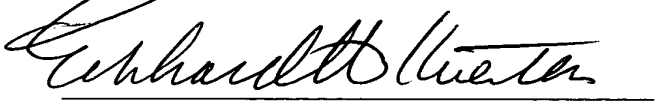

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